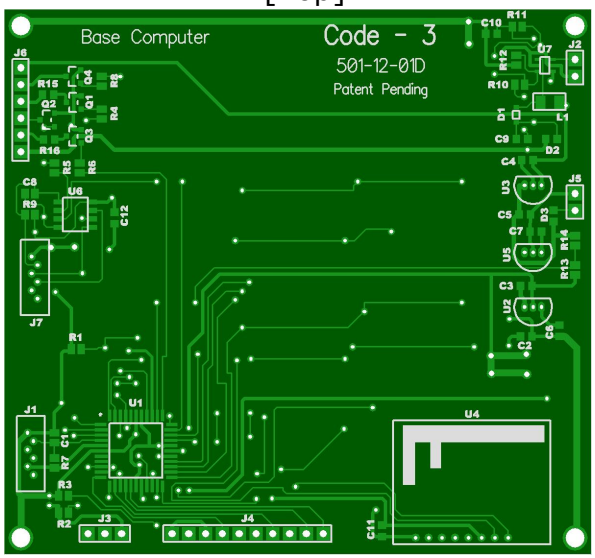
FAB3000 v8

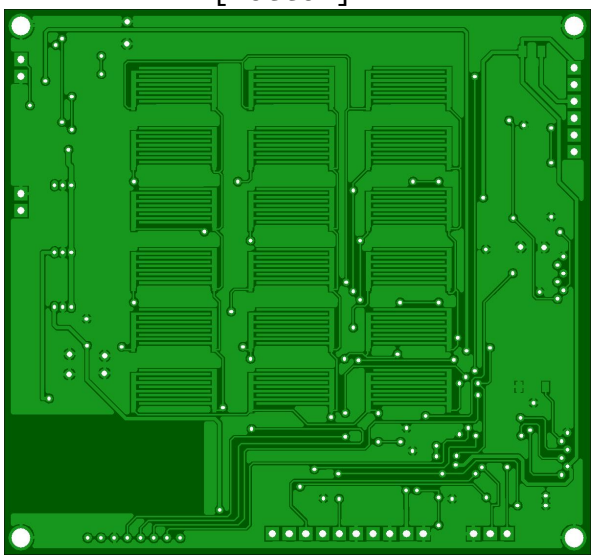
Date: 01/07/2019

DRC/DFM Check

[Top]



[Bottom]



DFM Summary (Bareboard):

Level: CRITICAL (20)
- Acid Traps: 20 violation(s)

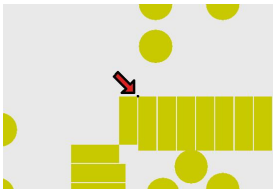
Level: ELEVATED (50)
- Mask Slivers: 25 violation(s)
- Silkscreen over Soldermask: 25 violation(s)

Level: MEDIUM (12)
- Minimum Width: Silkscreen Line: 12 violation(s)

Mask Slivers - (DFM Level: ELEVATED) Violation #: 1

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

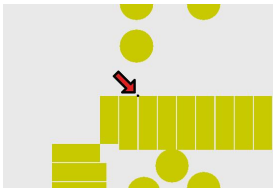
Layer: Top Mask.gbr Location: 1.045, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 2

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

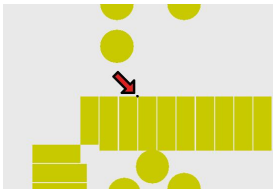
Layer: Top Mask.gbr Location: 1.076, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 3

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

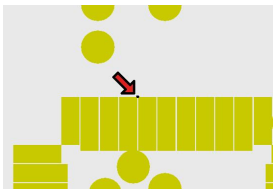
Layer: Top Mask.gbr Location: 1.108, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 4

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

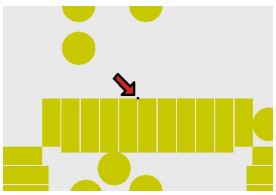
Layer: Top Mask.gbr Location: 1.139, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 5

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

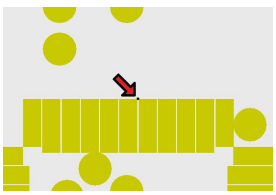
Layer: Top Mask.gbr Location: 1.171, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 6

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

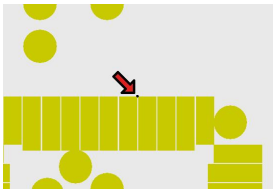
Layer: Top Mask.gbr Location: 1.202, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 7

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

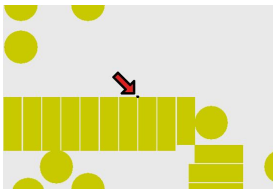
Layer: Top Mask.gbr Location: 1.234, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 8

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

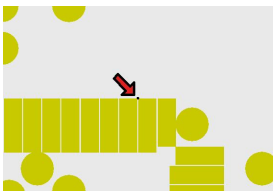
Layer: Top Mask.gbr Location: 1.265, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 9

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

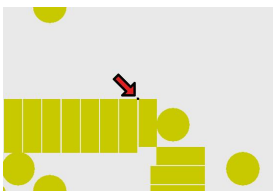
Layer: Top Mask.gbr Location: 1.297, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 10

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

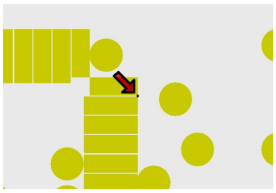
Layer: Top Mask.gbr Location: 1.328, 1.269 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 11

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

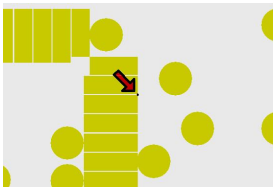
Layer: Top Mask.gbr Location: 1.438, 1.159 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 12

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

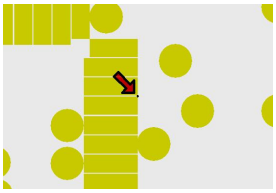
Layer: Top Mask.gbr Location: 1.438, 1.128 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 13

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

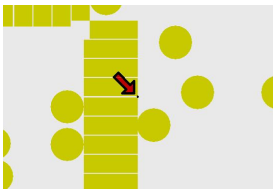
Layer: Top Mask.gbr Location: 1.438, 1.096 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 14

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

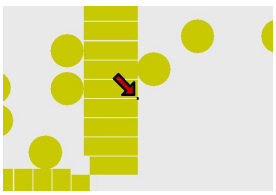
Layer: Top Mask.gbr Location: 1.438, 1.065 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 15

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

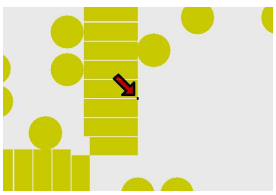
Layer: Top Mask.gbr Location: 1.438, 0.970 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 16

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

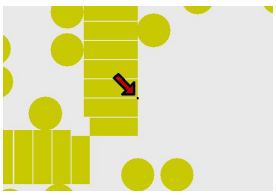
Layer: Top Mask.gbr Location: 1.438, 0.939 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 17

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

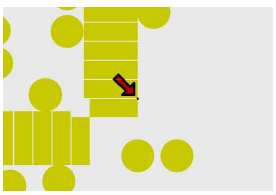
Layer: Top Mask.gbr Location: 1.438, 0.907 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 18

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

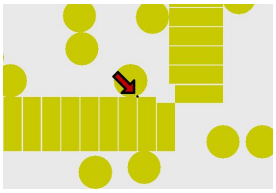
Layer: Top Mask.gbr Location: 1.438, 0.876 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 19

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

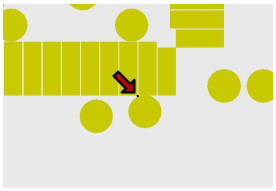
Layer: Top Mask.gbr Location: 1.297, 0.856 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 20

Clearance = 1.6 (mils), Minimum allowed 8.0 (mils).

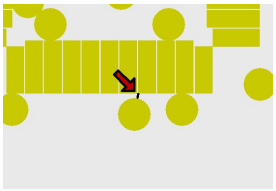
Layer: Top Mask.gbr Location: 1.296, 0.766 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 21

Clearance = 7.6 (mils), Minimum allowed 8.0 (mils).

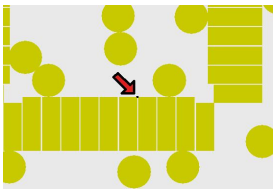
Layer: Top Mask.gbr Location: 1.234, 0.763 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 22

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

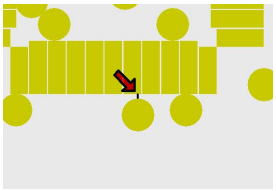
Layer: Top Mask.gbr Location: 1.234, 0.855 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 23

Clearance = 7.0 (mils), Minimum allowed 8.0 (mils).

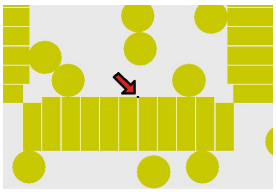
Layer: Top Mask.gbr Location: 1.227, 0.763 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 24

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

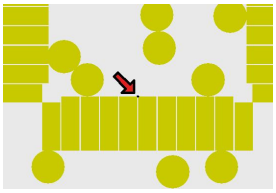
Layer: Top Mask.gbr Location: 1.202, 0.855 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Mask Slivers - (DFM Level: ELEVATED) Violation #: 25

Clearance = 1.8 (mils), Minimum allowed 8.0 (mils).

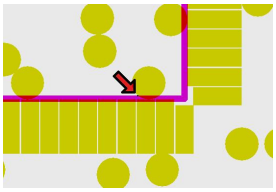
Layer: Top Mask.gbr Location: 1.171, 0.855 (in.)
Areas in the solder mask where the resist is so narrow that it may cause small pieces of the resist to flake off and present soldering problems later. Critical: A board can fail if the resist falls in an area that needs to be soldered later on.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 26

May make electrical testing & SMT soldering more difficult.

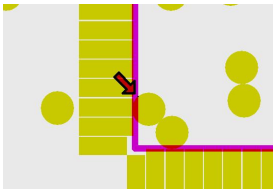
Layers: Top Silk.gbr, Top Mask.gbr Location: 1.268, 0.861 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 27

May make electrical testing & SMT soldering more difficult.

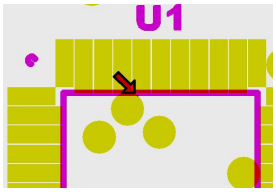
Layers: Top Silk.gbr, Top Mask.gbr Location: 1.032, 0.941 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 28

May make electrical testing & SMT soldering more difficult.

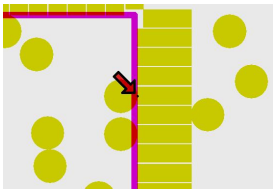
Layers: Top Silk.gbr, Top Mask.gbr Location: 1.149, 1.176 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 29

May make electrical testing & SMT soldering more difficult.

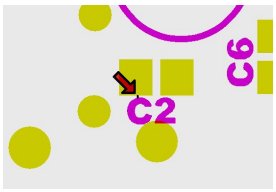
Layers: Top Silk.gbr, Top Mask.gbr Location: 1.350, 1.048 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 30

May make electrical testing & SMT soldering more difficult.

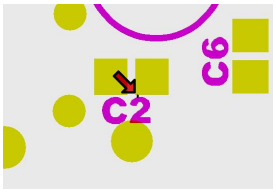
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.478, 1.668 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 31

May make electrical testing & SMT soldering more difficult.

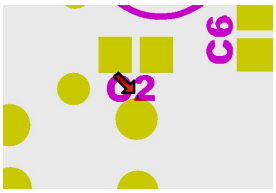
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.520, 1.668 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 32

May make electrical testing & SMT soldering more difficult.

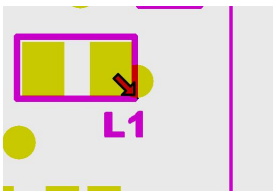
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.512, 1.631 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 33

May make electrical testing & SMT soldering more difficult.

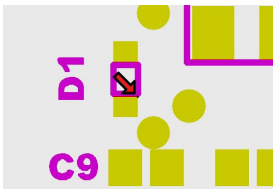
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.748, 3.049 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 34

May make electrical testing & SMT soldering more difficult.

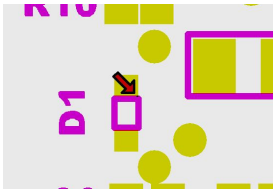
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.470, 2.991 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 35

May make electrical testing & SMT soldering more difficult.

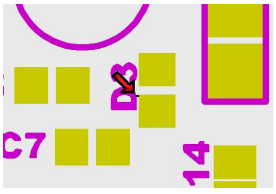
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.468, 3.048 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 36

May make electrical testing & SMT soldering more difficult.

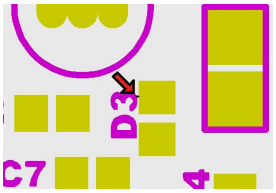
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.640, 2.409 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 37

May make electrical testing & SMT soldering more difficult.

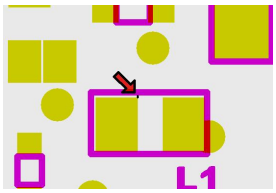
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.640, 2.454 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 38

May make electrical testing & SMT soldering more difficult.

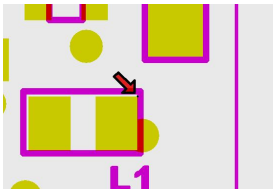
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.629, 3.142 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 39

May make electrical testing & SMT soldering more difficult.

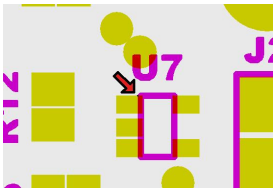
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.738, 3.140 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 40

May make electrical testing & SMT soldering more difficult.

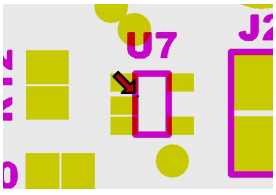
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.588, 3.365 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 41

May make electrical testing & SMT soldering more difficult.

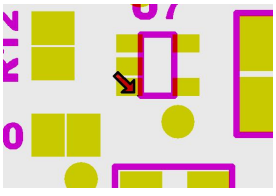
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.598, 3.327 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 42

May make electrical testing & SMT soldering more difficult.

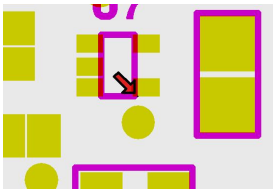
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.588, 3.264 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 43

May make electrical testing & SMT soldering more difficult.

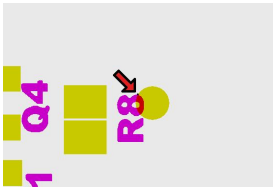
Layers: Top Silk.gbr, Top Mask.gbr Location: 3.654, 3.264 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 44

May make electrical testing & SMT soldering more difficult.

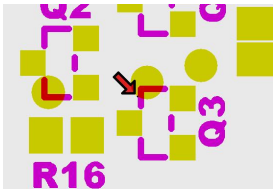
Layers: Top Silk.gbr, Top Mask.gbr Location: 1.068, 3.262 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 45

May make electrical testing & SMT soldering more difficult.

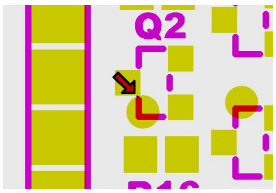
Layers: Top Silk.gbr, Top Mask.gbr Location: 0.784, 2.935 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 46

May make electrical testing & SMT soldering more difficult.

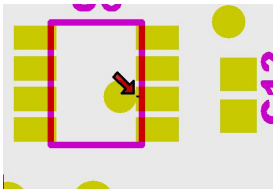
Layers: Top Silk.gbr, Top Mask.gbr Location: 0.629, 2.967 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 47

May make electrical testing & SMT soldering more difficult.

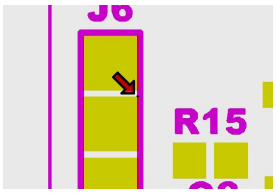
Layers: Top Silk.gbr, Top Mask.gbr Location: 0.893, 2.404 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 48

May make electrical testing & SMT soldering more difficult.

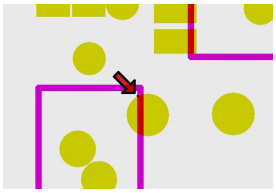
Layers: Top Silk.gbr, Top Mask.gbr Location: 0.544, 3.245 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 49

May make electrical testing & SMT soldering more difficult.

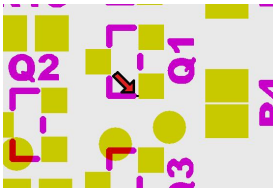
Layers: Top Silk.gbr, Top Mask.gbr Location: 0.663, 2.261 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Silkscreen over Soldermask - (DFM Level: ELEVATED) Violation #: 50

May make electrical testing & SMT soldering more difficult.

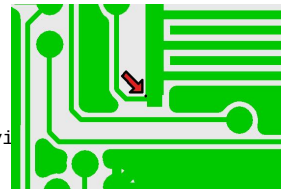
Layers: Top Silk.gbr, Top Mask.gbr Location: 0.836, 3.037 (in.)
The silkscreen overlaps solder mask openings. Elevated Risk: May cause contamination of the pads and make electrical testing plus SMT soldering more difficult.



Acid Traps - (DFM Level: CRITICAL) Violation #: 51

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

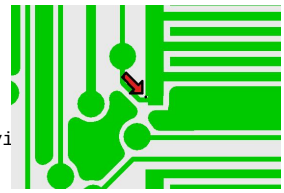
Layer: Bottom.gbr Location: 1.232, 1.265 (in.)
Attributes: Net=$Net00009
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 52

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

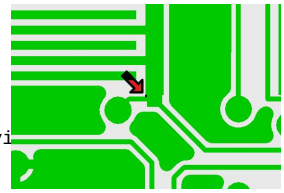
Layer: Bottom.gbr Location: 1.232, 1.625 (in.)
Attributes: Net=$Net00009
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 53

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

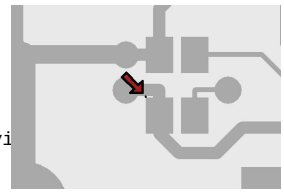
Layer: Bottom.gbr Location: 1.714, 1.265 (in.)
Attributes: Net=$Net00028
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 54

Gap = 2.0 (mils), Minimum allowed 7.0 (mils).

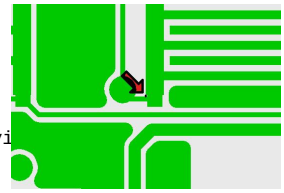
Layer: Top.gbr Location: 0.702, 0.681 (in.)
Attributes: Net=$Net00004
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 55

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

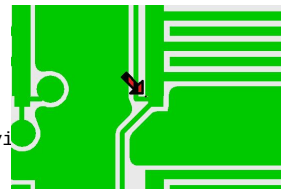
Layer: Bottom.gbr Location: 2.632, 1.265 (in.)
Attributes: Net=$Net00022
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 56

Gap = 0.5 (mils), Minimum allowed 7.0 (mils).

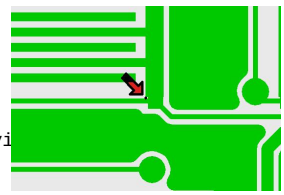
Layer: Bottom.gbr Location: 2.632, 1.626 (in.)
Attributes: Net=$Net00022
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 57

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

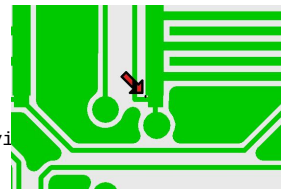
Layer: Bottom.gbr Location: 2.414, 1.265 (in.)
Attributes: Net=$Net00028
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 58

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

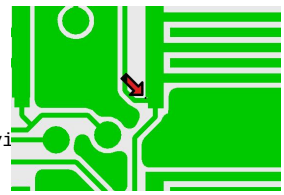
Layer: Bottom.gbr Location: 1.932, 1.265 (in.)
Attributes: Net=$Net00026
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 59

Gap = 0.5 (mils), Minimum allowed 7.0 (mils).

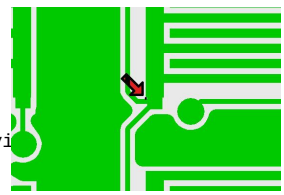
Layer: Bottom.gbr Location: 1.932, 1.626 (in.)
Attributes: Net=$Net00026
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 60

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

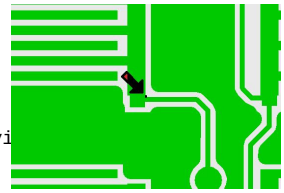
Layer: Bottom.gbr Location: 2.632, 2.345 (in.)
Attributes: Net=$Net00022
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 61

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

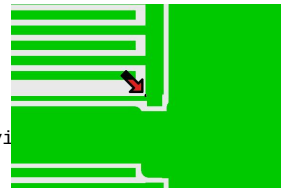
Layer: Bottom.gbr Location: 2.444, 1.985 (in.)
Attributes: Net=$Net00020
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 62

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

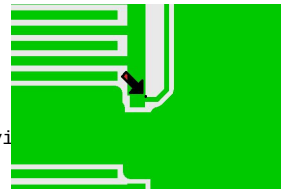
Layer: Bottom.gbr Location: 3.114, 2.345 (in.)
Attributes: Net=$Net00011
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 63

Gap = 2.5 (mils), Minimum allowed 7.0 (mils).

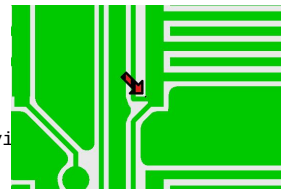
Layer: Bottom.gbr Location: 3.144, 3.065 (in.)
Attributes: Net=$Net00013
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 64

Gap = 0.5 (mils), Minimum allowed 7.0 (mils).

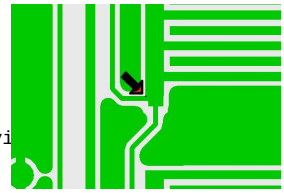
Layer: Bottom.gbr Location: 1.932, 2.706 (in.)
Attributes: Net=$Net00026
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 65

Gap = 0.5 (mils), Minimum allowed 7.0 (mils).

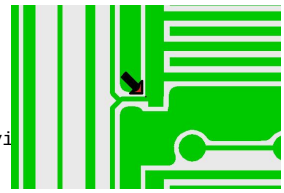
Layer: Bottom.gbr Location: 1.232, 2.346 (in.)
Attributes: Net=$Net00009
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) Violation #: 66

Gap = 0.5 (mils), Minimum allowed 7.0 (mils).

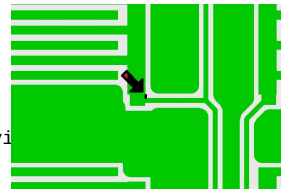
Layer: Bottom.gbr Location: 1.232, 2.706 (in.)
Attributes: Net=$Net00009
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) — Violation #: 67

Gap = 6.4 (mils), Minimum allowed 7.0 (mils).

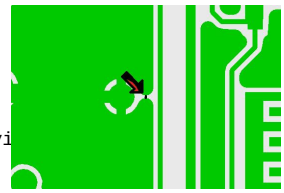
Layer: Bottom.gbr Location: 1.744, 3.063 (in.)
Attributes: Net=$Net00013
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) — Violation #: 68

Gap = 4.1 (mils), Minimum allowed 7.0 (mils).

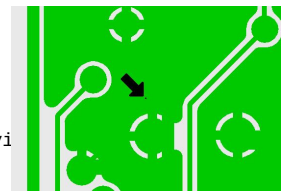
Layer: Bottom.gbr Location: 1.068, 2.218 (in.)
Attributes: Net=$Net00004
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) — Violation #: 69

Gap = 0.1 (mils), Minimum allowed 7.0 (mils).

Layer: Bottom.gbr Location: 0.670, 2.292 (in.)
Attributes: Net=$Net00004
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi



Acid Traps - (DFM Level: CRITICAL) — Violation #: 70

Gap = 5.0 (mils), Minimum allowed 7.0 (mils).

Layer: Bottom.gbr Location: 0.840, 2.956 (in.)
Attributes: Net=$Net00004
Due to the surface tension during the etching process, larger deposits of acid may get trapped into certain areas - resulting in over-etching. Critical: Over-etching will directly effect your board yi

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) — Violation #: 71

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.405, 3.189 (in.)
This object may not be visible on the silkscreen.

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) — Violation #: 72

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.448, 3.165 (in.)
This object may not be visible on the silkscreen.

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 73

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.478, 3.145 (in.)
This object may not be visible on the silkscreen.

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 74

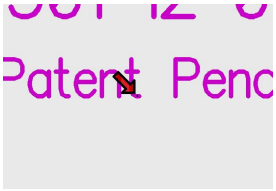
Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.535, 3.165 (in.)
This object may not be visible on the silkscreen.

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 75

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.593, 3.145 (in.)
This object may not be visible on the silkscreen.



Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 76

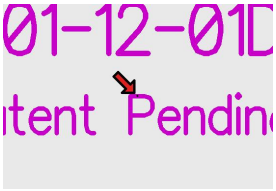
Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.691, 3.189 (in.)
This object may not be visible on the silkscreen.

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 77

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

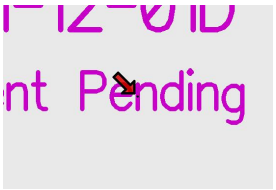
Layer: Top Silk.gbr Location: 2.667, 3.205 (in.)
This object may not be visible on the silkscreen.



Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 78

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.746, 3.165 (in.)
This object may not be visible on the silkscreen.



Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 79

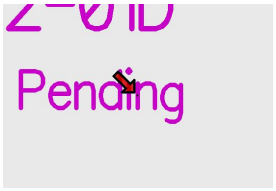
Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.832, 3.165 (in.)
This object may not be visible on the silkscreen.

Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 80

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

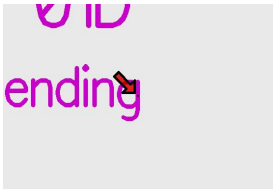
Layer: Top Silk.gbr Location: 2.846, 3.165 (in.)
This object may not be visible on the silkscreen.



Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 81

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.917, 3.159 (in.)
This object may not be visible on the silkscreen.



Minimum Width: Silkscreen Line - (DFM Level: MEDIUM) Violation #: 82

Silkscreen Width = 6.6 (mils), Minimum allowed 7.0 (mils).

Layer: Top Silk.gbr Location: 2.381, 3.205 (in.)
This object may not be visible on the silkscreen.